

TECHNICAL JOURNAL

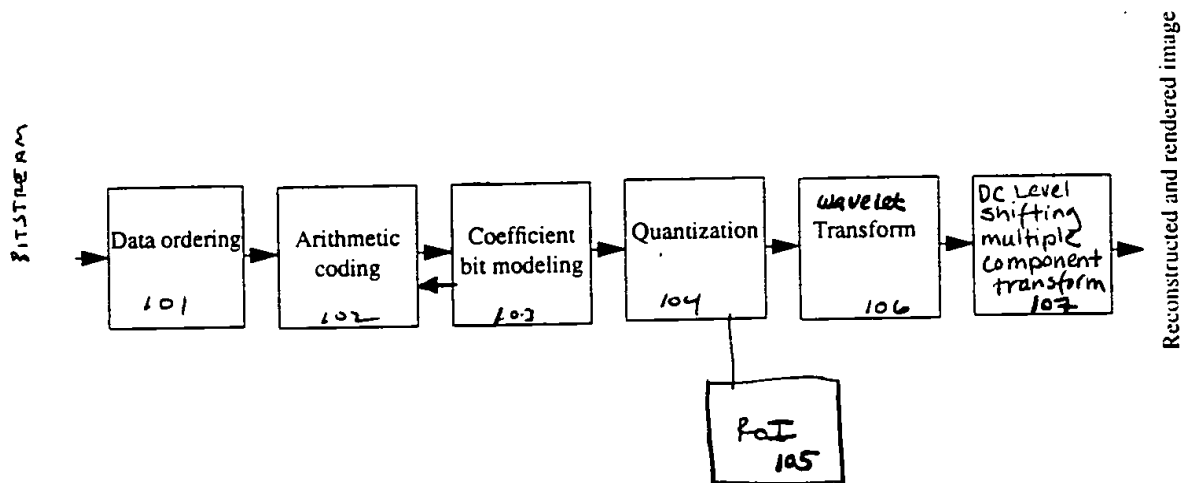


Figure 1

Figure 2A

SP 0	SP 4	C 8	C 12	C 16	C 20	C 24	C 28
R 1	SP 5	C 9	C 13	C 17	C 21	C 25	C 29
R 2	SP 6	SP 10	SP 14	SP 18	C 22	C 26	C 30
SP 3	SP 7	R 11	R 15	SP 19	C 23	C 27	C 31
C 32	SP 36	SP 40	SP 44	SP 48	C 52	C 56	C 60
C 33	C 37	C 41	C 45	C 49	C 53	C 57	C 61
C 34	C 38	C 42	C 46	C 50	C 54	C 58	C 62
C 25	C 39	C 43	C 47	C 51	C 55	C 59	C 63

Figure 2A

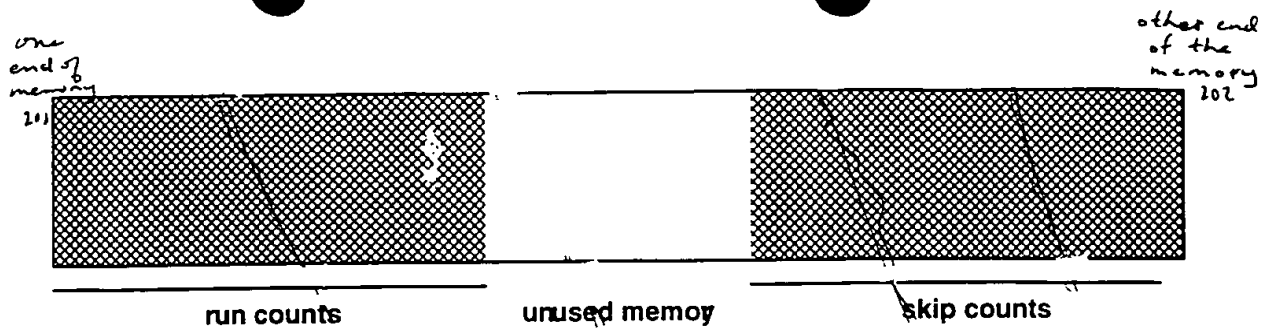


Figure 2B

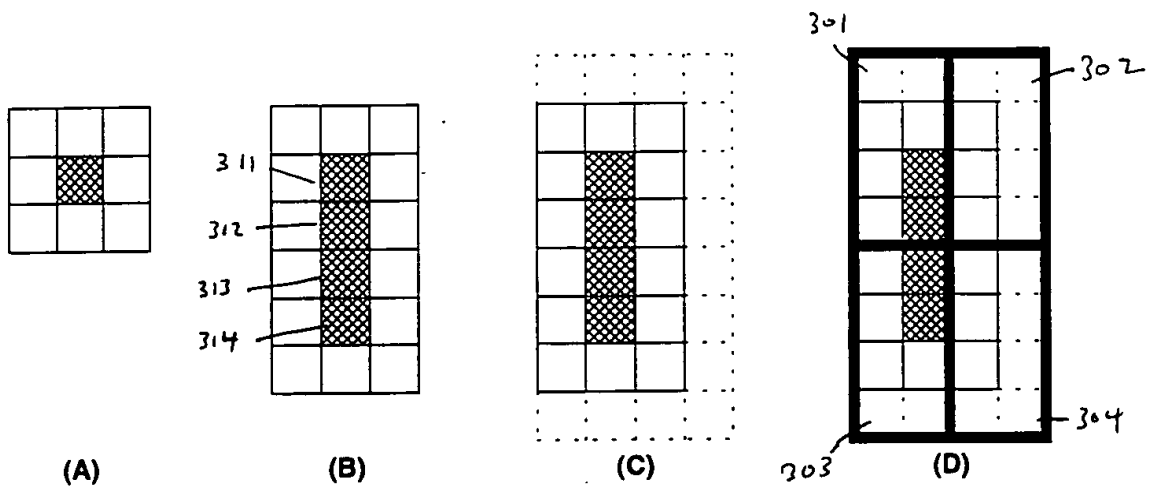
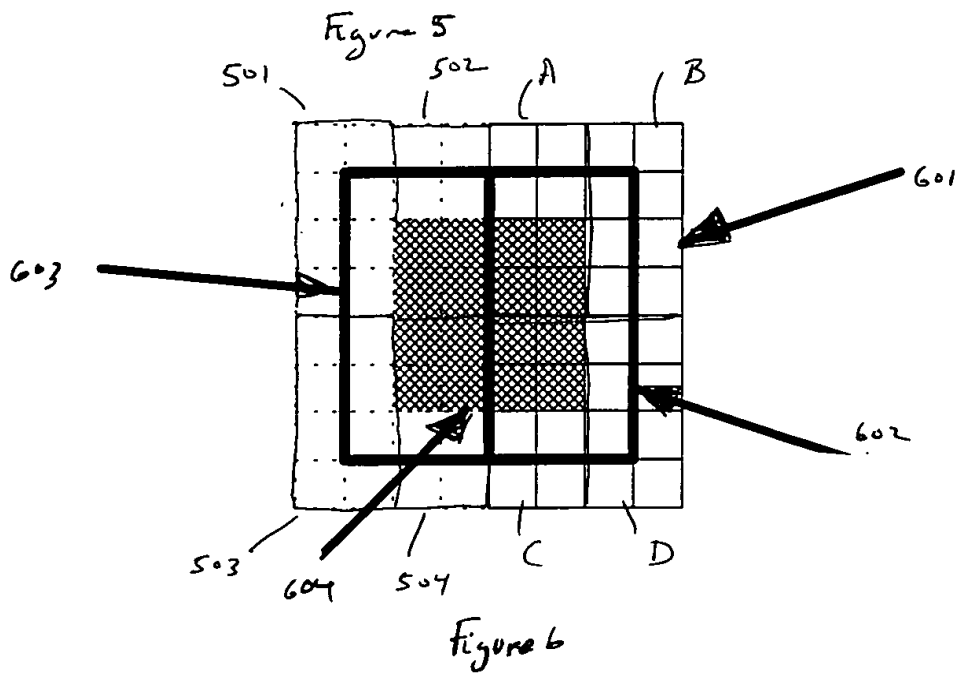
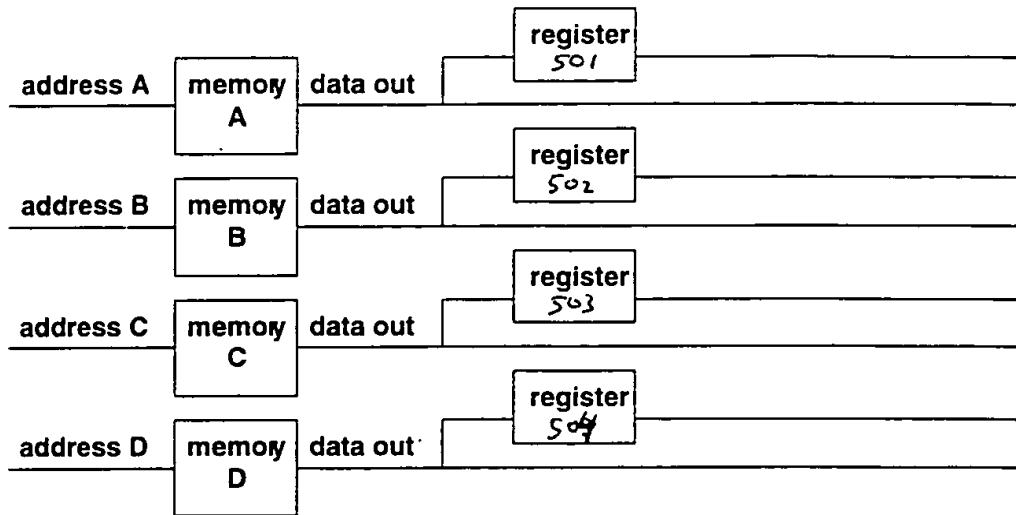


Figure 3

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	0	1	2	3	4	5	6	7
0	A	B	A	B	A	B	A	B
1	C	D	C	D	C	D	C	D
2	A	B	A	B	A	B	A	B
3	C	D	C	D	C	D	C	D
0	A	B	A	B	A	B	A	B

Figure 4



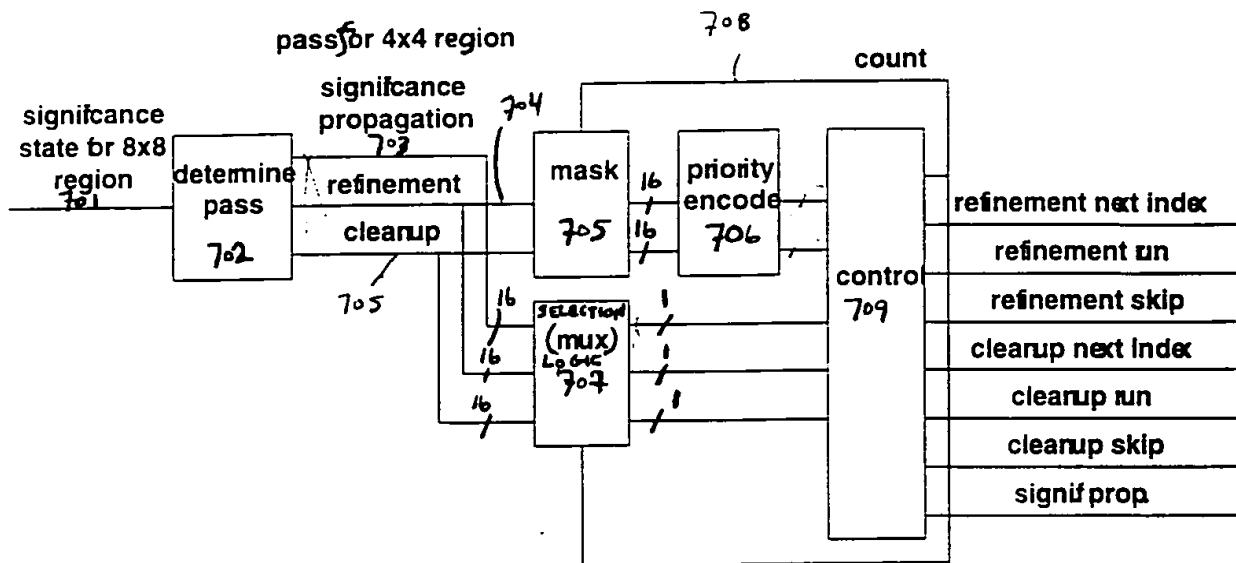


Figure 7

SP	SP	SP	SP
C	C	C	C
SP	SP	SP	SP
SP	R	R	SP

SP = significance propagation
C = cleanup
R = refinement

SP pass: 10*2 for SP pass coefficients
6 for C and R pass coefficients
C pass: 4*2 for C pass coefficients
R pass: 2 for R pass

total: 36 clocks = 2.25 clocks per coefficient

Figure 8

	0	1	2	3
0	A	A	A	A
1	B	B	B	B
2	A	A	A	A
3	B	B	B	B
0	A	A	A	A

Figure 9

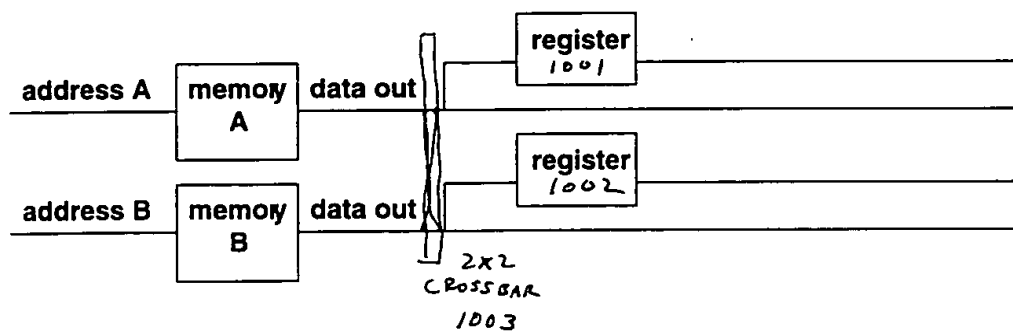


Figure 10

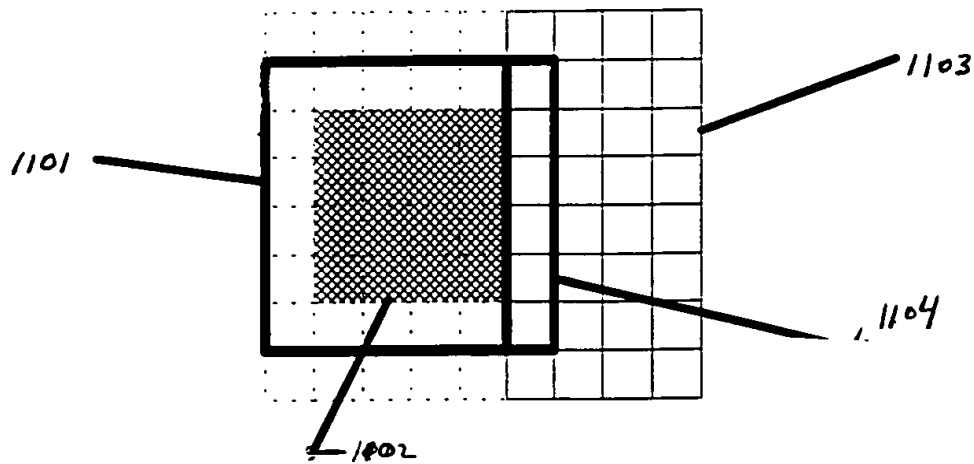


Figure 11

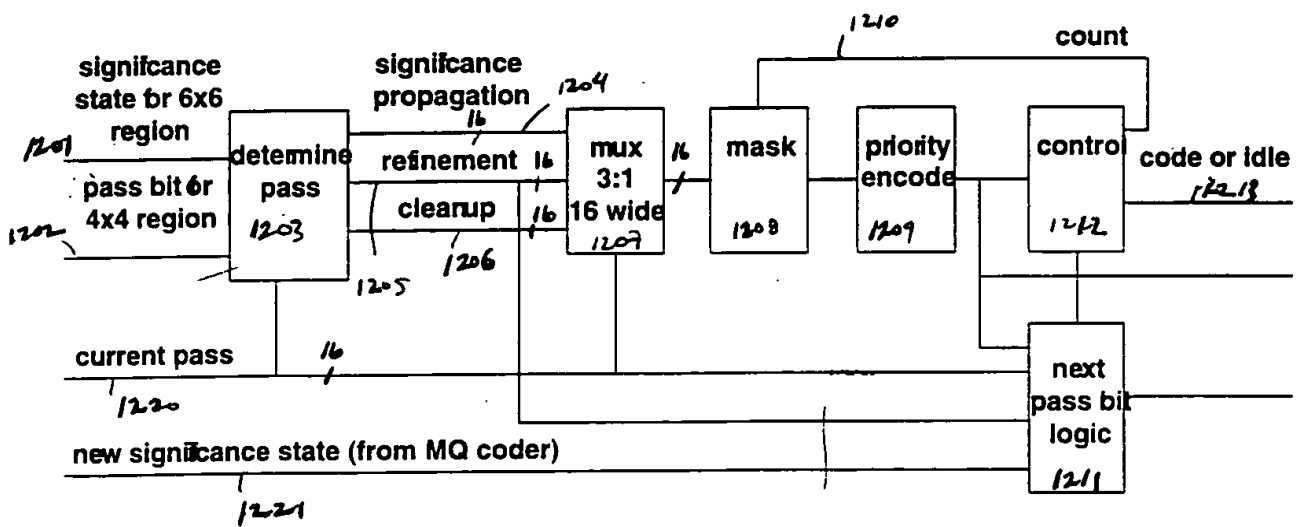


Figure 12

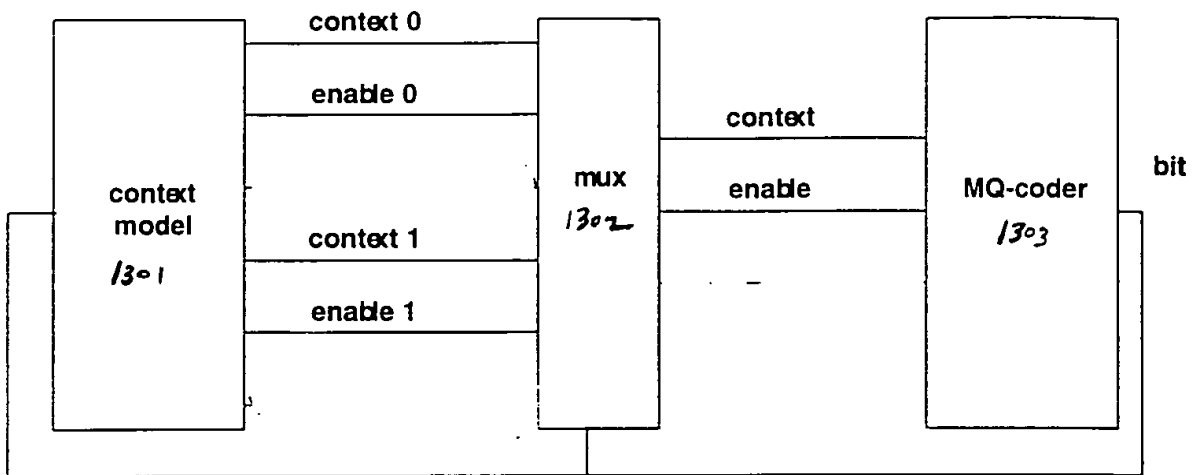


Figure 13

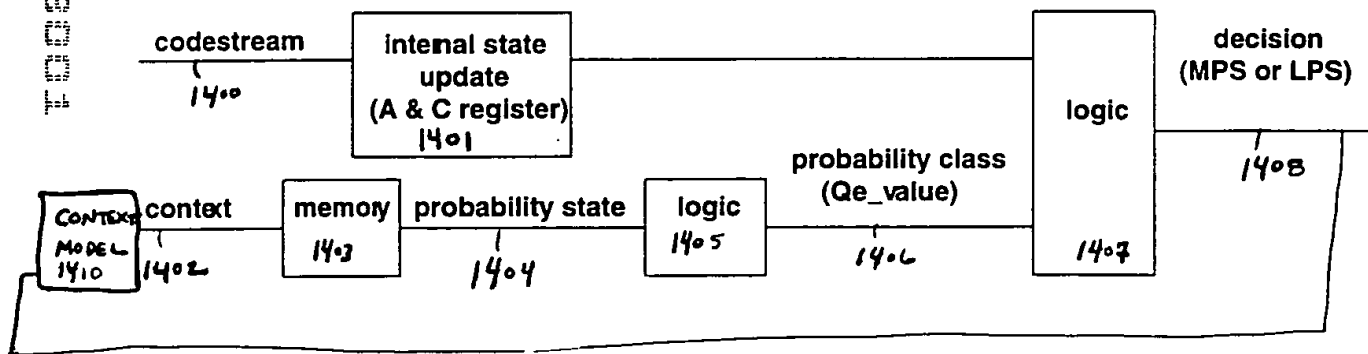


Figure 14A

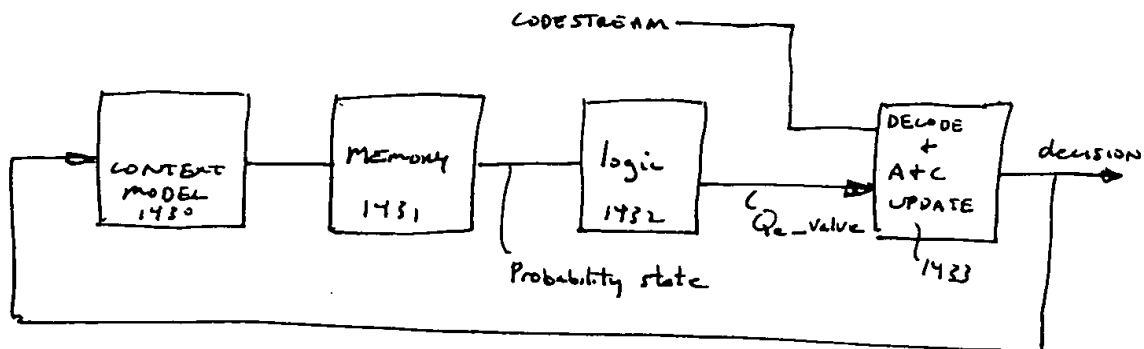


Figure 14B

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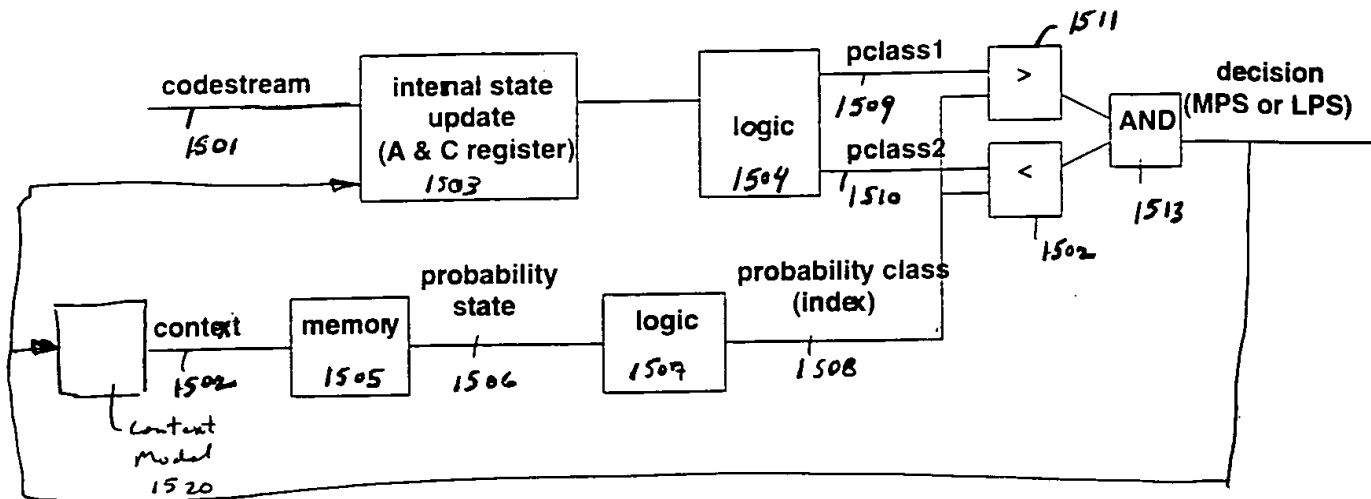


Figure 15

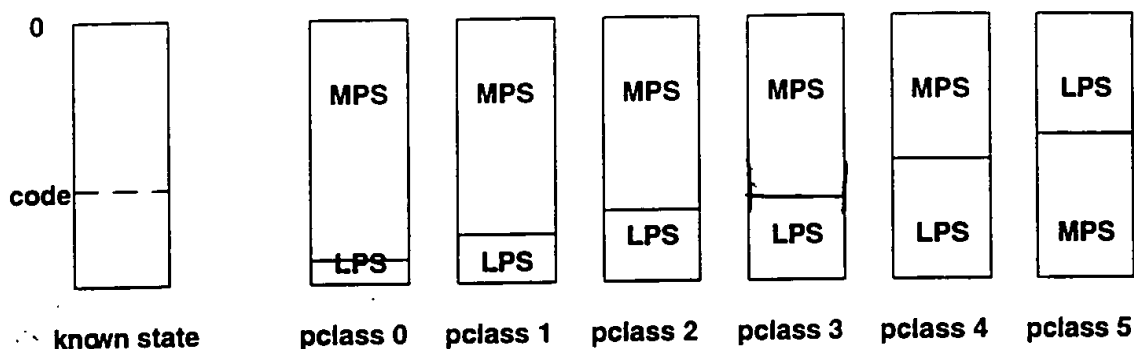


Figure 16A

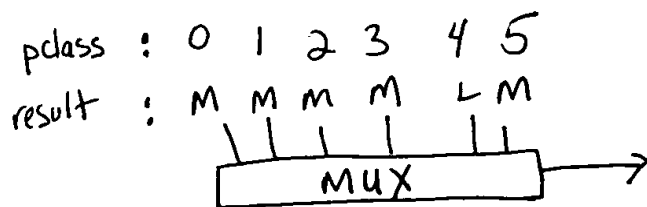


Figure 16B

5MPS
4 MPS
3 MPS
2 MPS
1 MPS
LPS

Figure 17

luminance				chrominance				chrominance			
A	A	A	D	B	B	B	D	C	C	C	D
A	A			B	B			C	C		
A		A		B		B		C		C	
A				B				C			

(A)

A	A	A	B
A	A		
A		A	
B			

C	C	C	D
C	C		
C		C	
D			

E	E	E	F
E	E		
E		E	
F			

(B)

F	F	B	C
F	F		
A		A	
A			
B			

G	G	C	F
G	G		
B		C	
D			
H			

E	E	E	E
E	E		
D		D	
G			
H			

(C)

Figure 18

TOP SECRET

luminance				chrominance				chrominance			
A	A	A	B	C	C	C		D	D	D	
A	A			C	C			D	D		
A		A		C	C	D		D			
B				A							

(A)

F	F	F	C
A	A		
F		F	
A			

B	B	C	
C	C		
A		B	
D			

D	D	F	
E	E		
D		E	
E			

(B)

A	A	A	C
A	A		
A		A	
B			

E	E	E	
E	E		
E		E	
F			

G	G	G	
G	G		
G		G	
H			

(C)

Figure 19

TOP SECRET

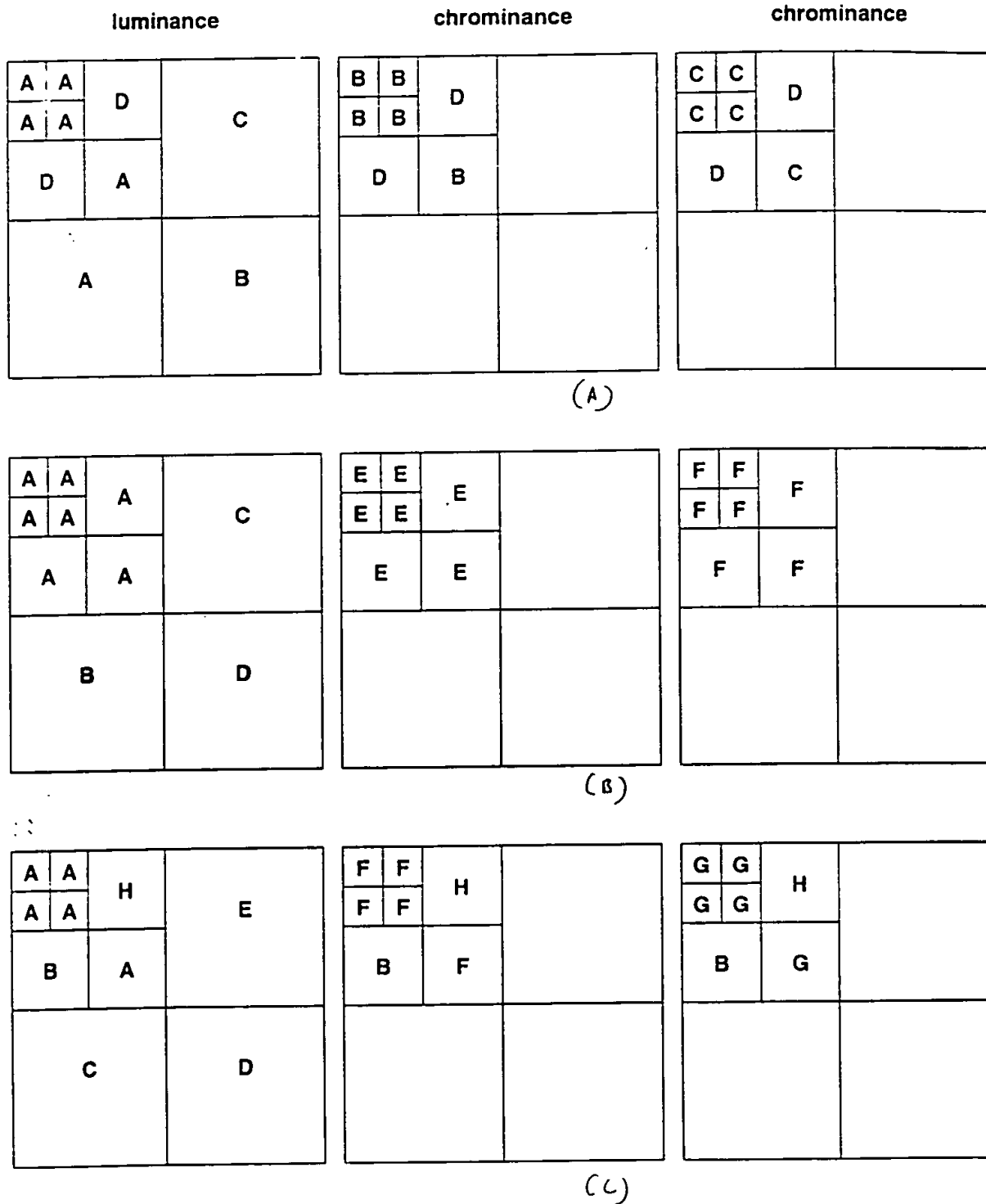


Figure 20

The diagram illustrates a memory architecture for a video encoder. It consists of a vertical stack of four memory blocks. Each block contains two distinct regions: a top region with a cross-hatch pattern labeled 'coded data' and a bottom region with a vertical-line pattern labeled 'length, zero bitplanes and coding passes'. A bracket on the right side of the stack is labeled 'workspace memory'. The bottom of the stack is labeled 'coded data memor (or memories)'.

Fig 21

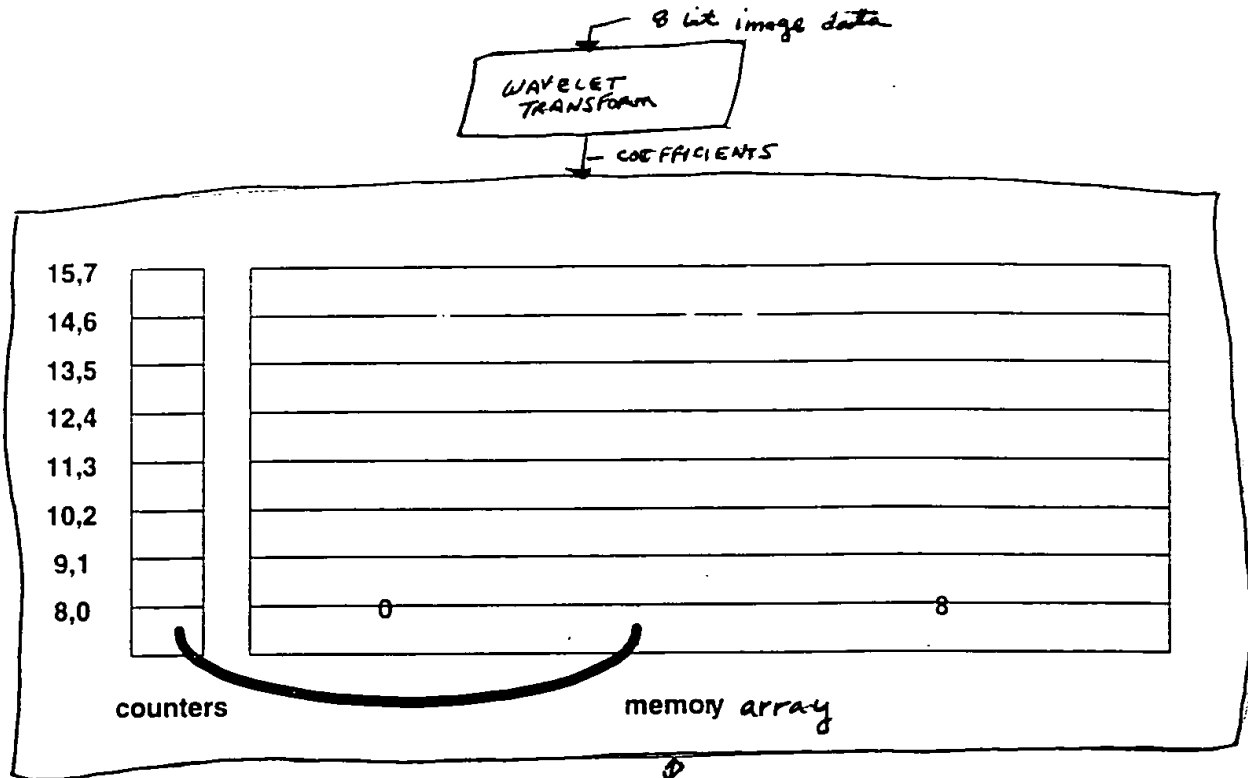


Figure 22A

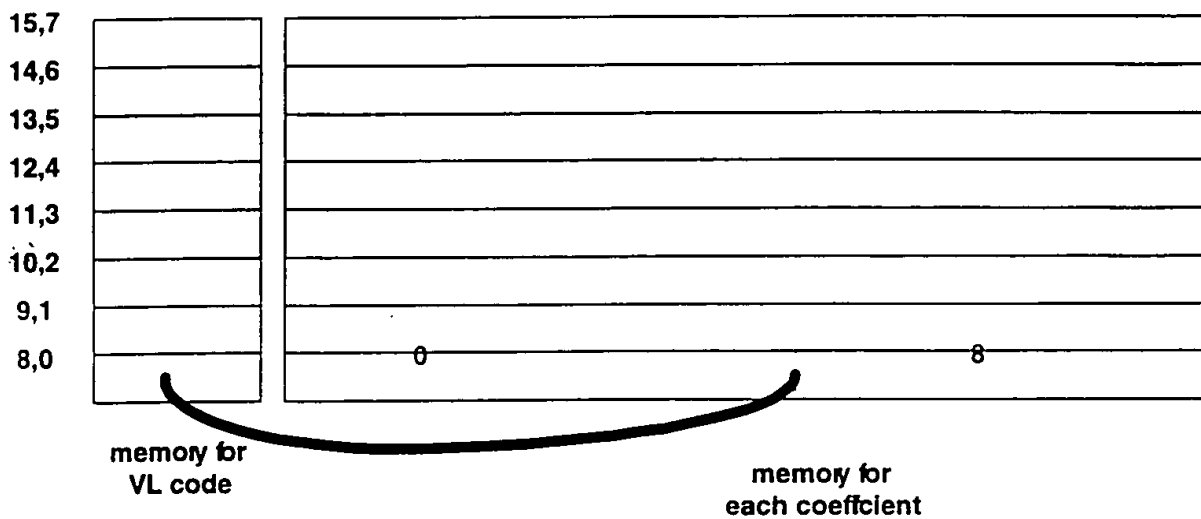
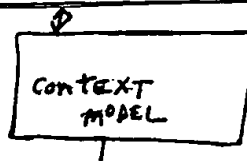


Figure 23

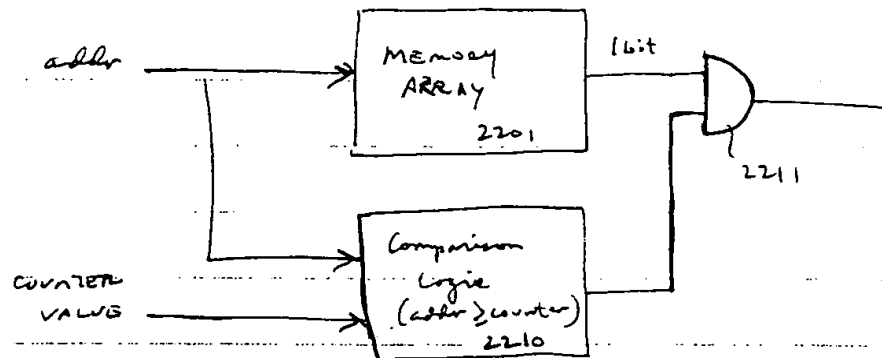
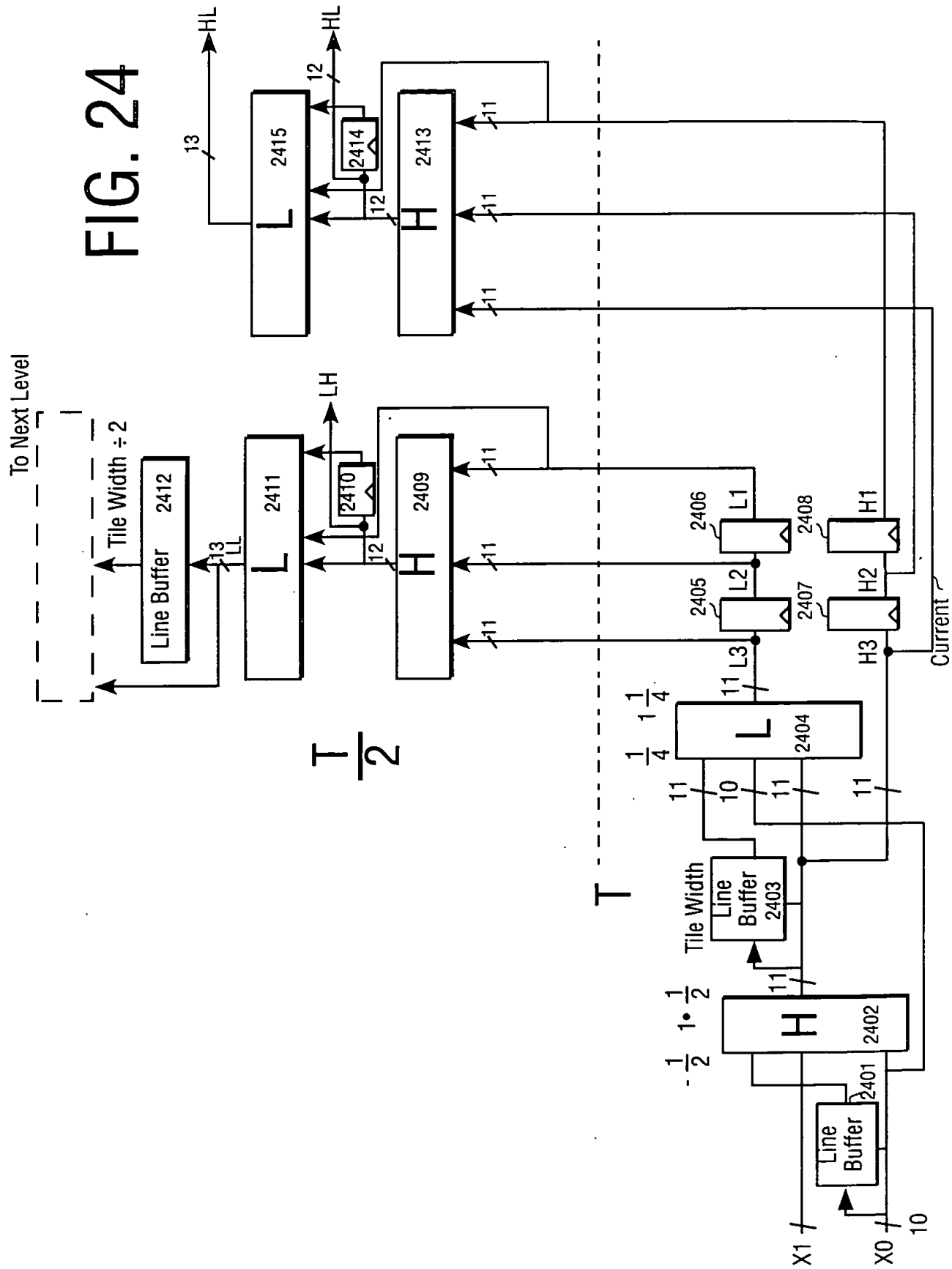


Figure 22B

FIG. 24



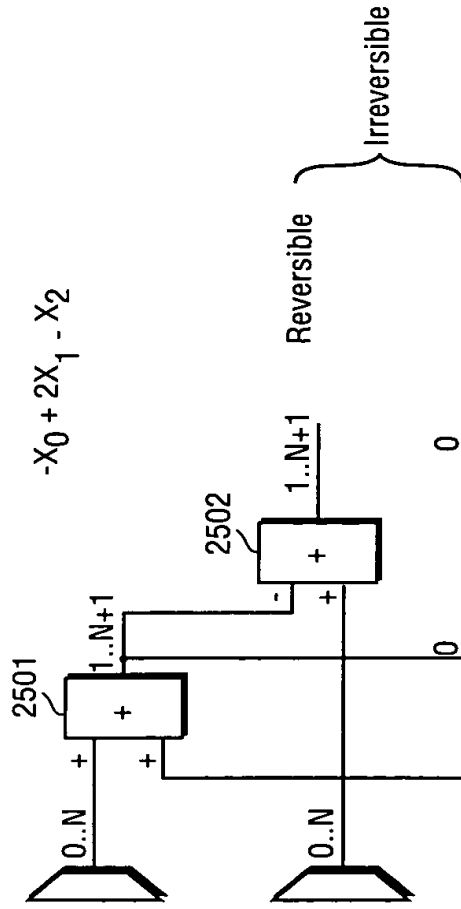
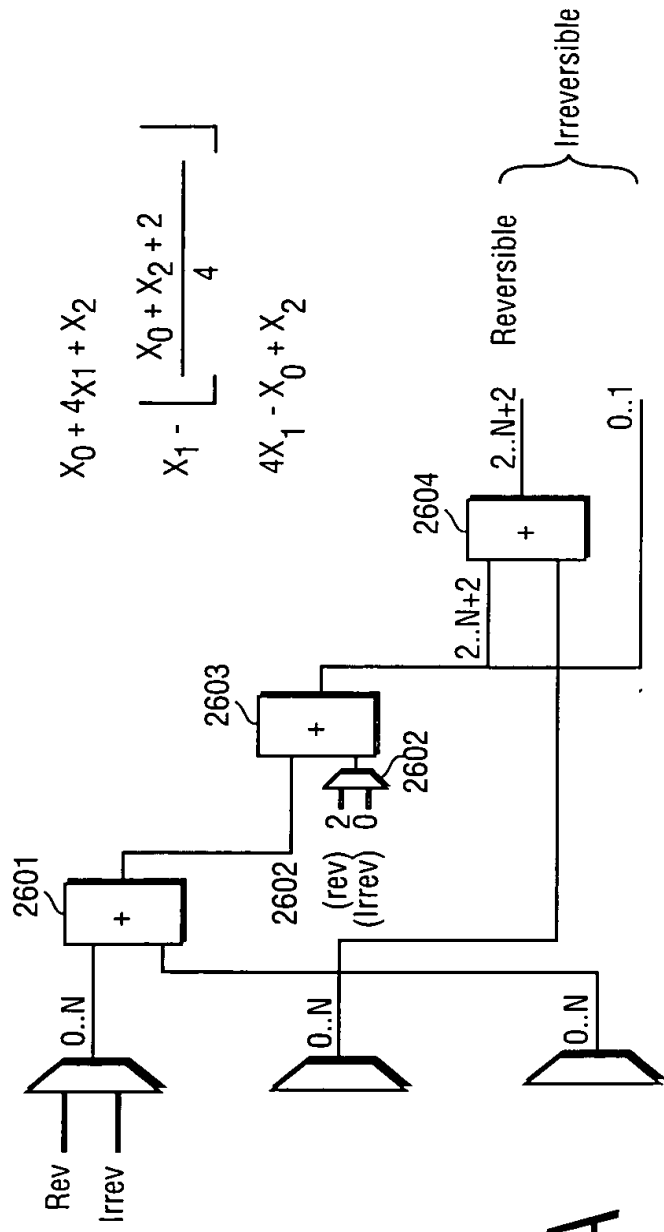


FIG. 25A



$$X_0 + 4X_1 + X_2$$

$$X_1 - \left[\frac{X_0 + X_2 + 2}{4} \right]$$

$$4X_1 - X_0 + X_2$$

FIG. 26A

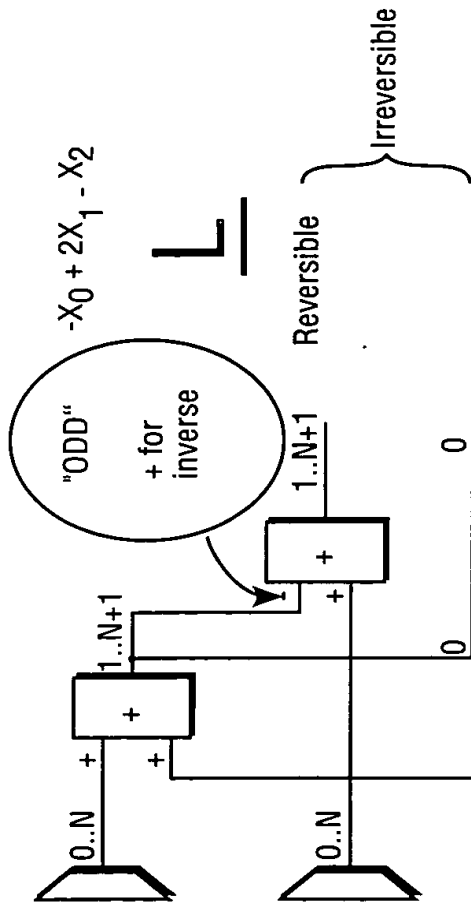


FIG. 25B

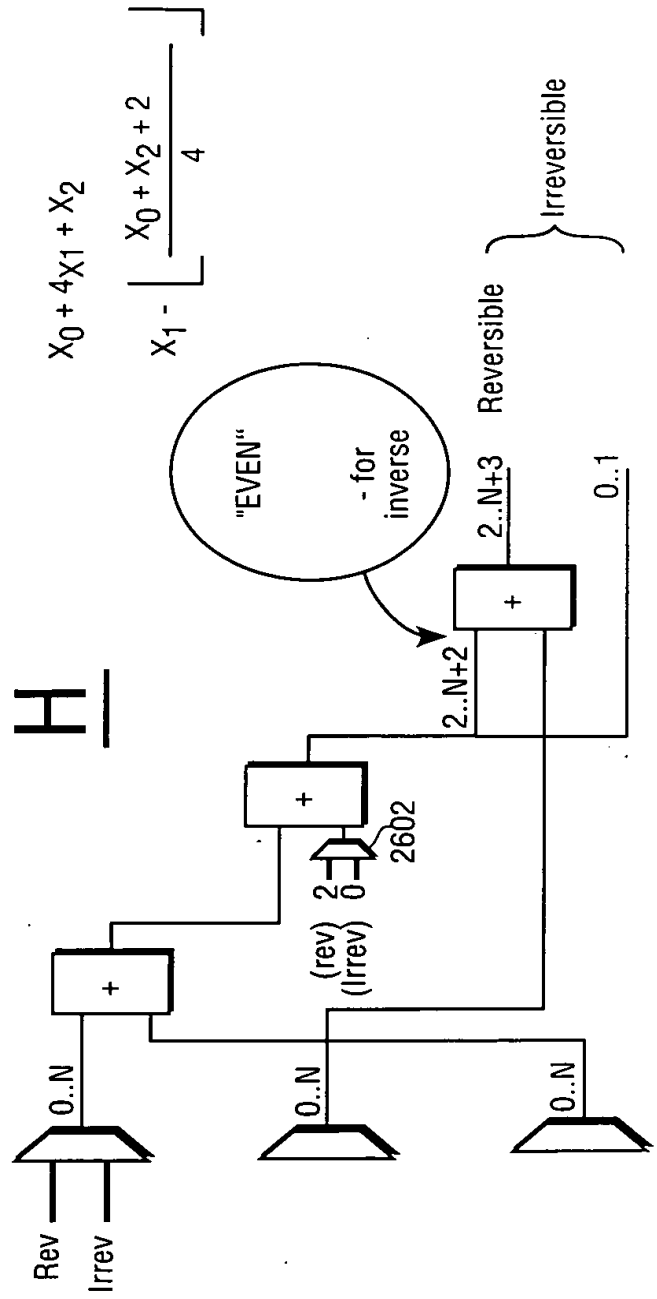
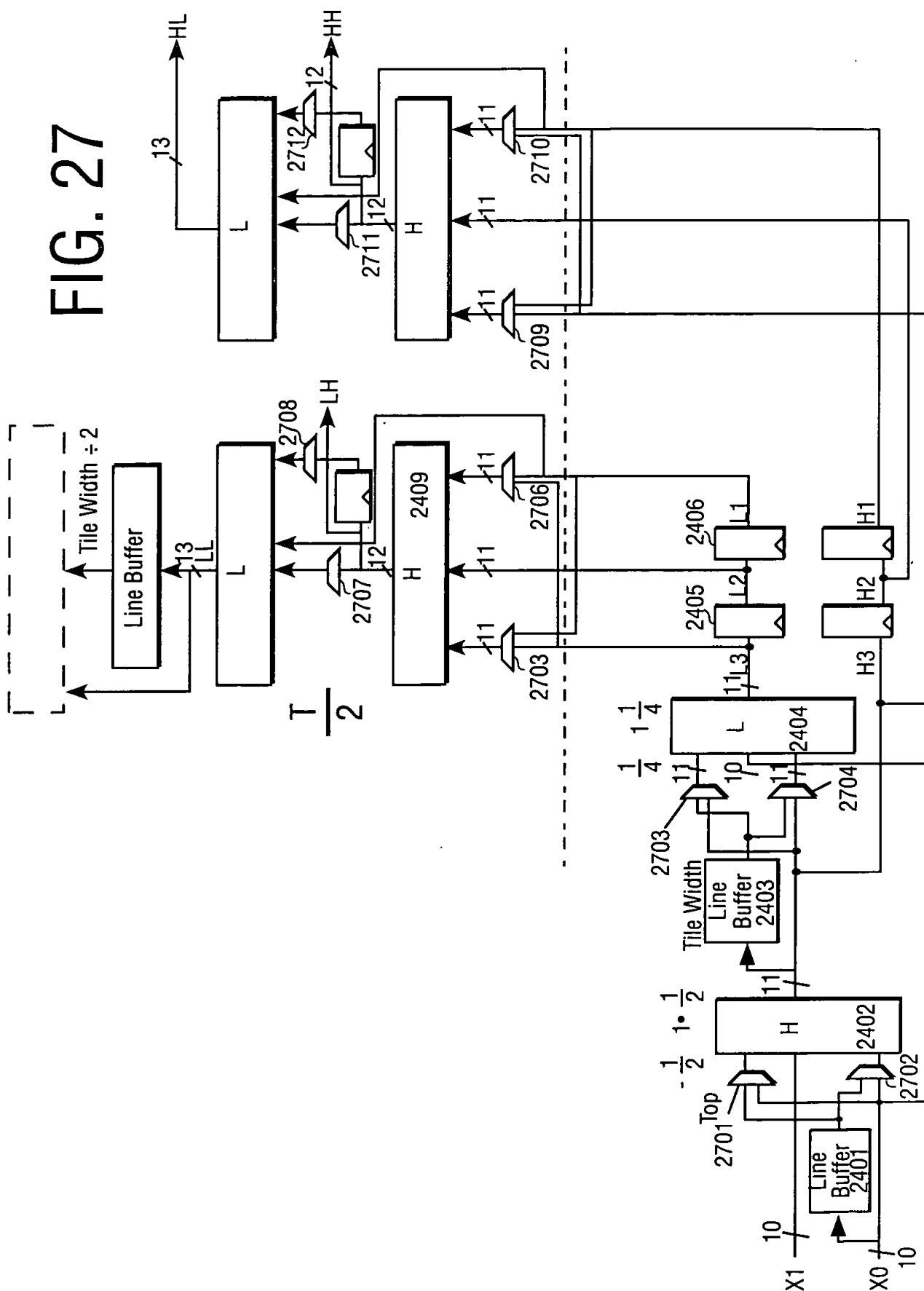


FIG. 26B

FIG. 27



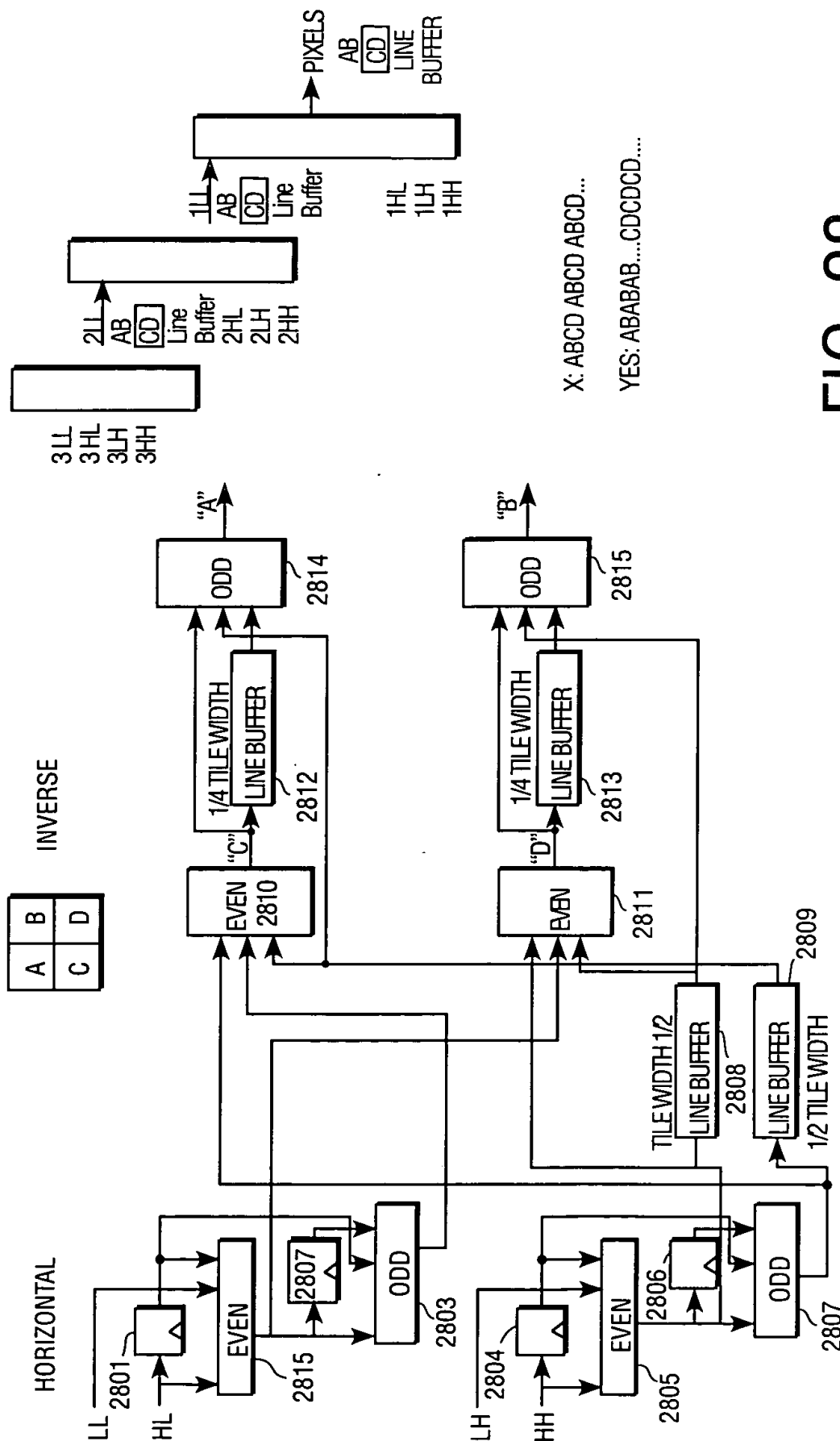


FIG. 28

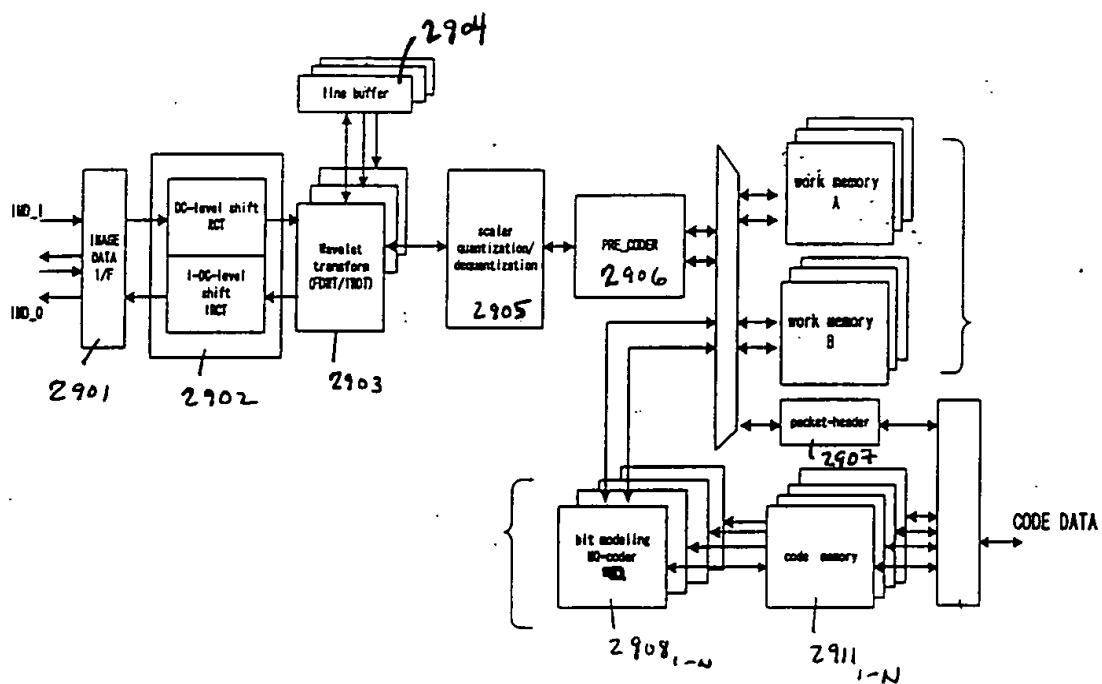


Figure 29

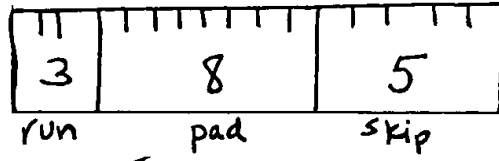


Figure 30

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Year	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

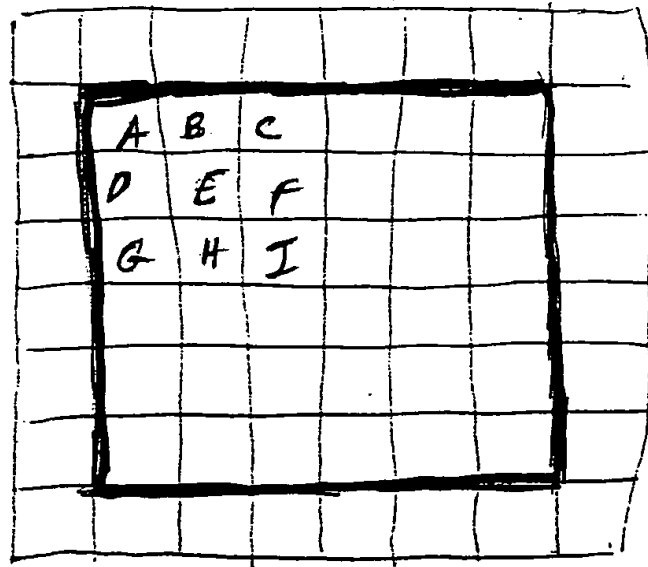


Figure 31

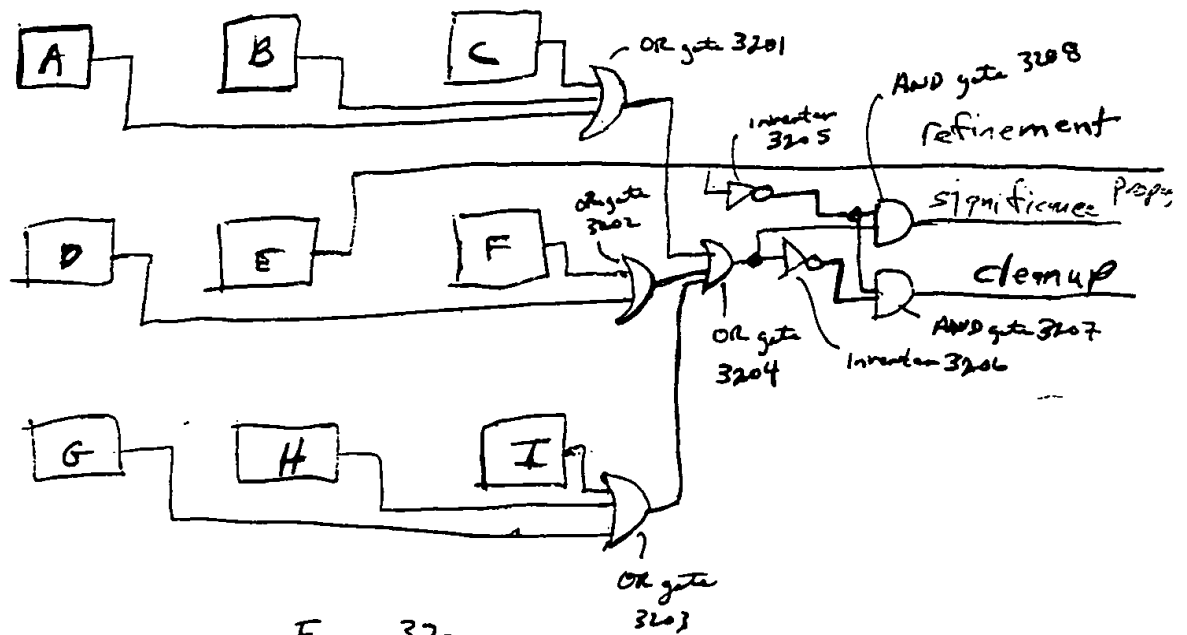


Figure 32